

We claim:

1           1.     A data slicer comprising:  
2           a first comparator circuit that establishes a first threshold;  
3           a second comparator circuit that establishes a second threshold; and  
4           a third comparator circuit that establishes a third threshold;  
5           wherein the second threshold is greater than the first threshold and less than  
6 the third threshold,  
7           wherein each of the comparator circuits has an offset, and  
8           wherein the first and third comparator circuits have symmetrical offsets.

1           2.     The data slicer of claim 1 wherein the first and third comparator circuits  
2 have output circuits providing the symmetrical offsets.

1           3.     The data slicer of claim 1 wherein each of the first and third comparator  
2 circuits includes a load resistor having a center tap and wherein the load resistor  
3 center tap of the first comparator circuit is coupled to the load resistor center tap of  
4 the third comparator circuit to provide the first and second comparator circuits with  
5 symmetrical offsets.

1           4.     The data slicer of claim 1 wherein the first and third thresholds are  
2 equally spaced from the second threshold.

1           5.     The data slicer of claim 1 wherein the comparator circuits are formed  
2 from complimentary metal oxide semiconductor devices.

1           6.     A data slicer comprising:  
2           a first comparator circuit that establishes a first threshold;  
3           a second comparator circuit that establishes a second threshold; and  
4           a third comparator circuit that establishes a third threshold;  
5           wherein the second threshold is greater than the first threshold and less than  
6 the third threshold,  
7           wherein each of the comparator circuits has an offset, and  
8           wherein the first and third comparator circuits have output circuits providing  
9 symmetrical offsets.

1           7.     The data slicer of claim 6 wherein the output circuit of each of the first  
2     and third comparator circuits includes a load resistor having a center tap and wherein  
3     the load resistor center tap of the first comparator circuit is coupled to the load  
4     resistor center tap of the third comparator circuit to provide the first and second  
5     comparator circuits with the symmetrical offsets.

1           8.     The data slicer of claim 6 wherein the first and third thresholds are  
2     equally spaced from the second threshold.

1           9.     The data slicer of claim 6 wherein the comparator circuits are formed  
2     from complimentary metal oxide semiconductor devices.

1           10.    A data slicer comprising:  
2           a first comparator circuit that establishes a first threshold;  
3           a second comparator circuit that establishes a second threshold; and  
4           a third comparator circuit that establishes a third threshold,  
5           wherein the second threshold is greater than the first threshold and less than  
6     the third threshold,  
7           wherein the first and third comparator circuits each includes a load resistor  
8     having a center tap, and  
9           wherein the load resistor center tap of the first comparator circuit is coupled to  
10    the load resistor center tap of the third comparator circuit.

1           11.    The data slicer of claim 10 wherein the first and third thresholds are  
2     equally spaced from the second threshold.

1           12.    The data slicer of claim 10 wherein the comparator circuits are formed  
2     from complimentary metal oxide semiconductor devices.

1           13.    An integrated circuit comprising:  
2           a substrate of semiconductor material; and  
3           a data slicer formed in the semiconductor material, the data slicer including,  
4           a first comparator circuit that establishes a first threshold,  
5           a second comparator circuit that establishes a second threshold, and  
6           a third comparator circuit that establishes a third threshold,

7            wherein the second threshold is greater than the first threshold and less than  
8 the third threshold,

9            wherein each of the comparator circuits has an offset, and

10           wherein the first and third comparator circuits have symmetrical offsets.

1           14.    The integrated circuit of claim 13 wherein the first and third comparator  
2 circuits have output circuits providing the symmetrical offsets.

1           15.    The integrated circuit of claim 13 wherein each of the first and third  
2 comparator circuits includes a load resistor having a center tap and wherein the load  
3 resistor center tap of the first comparator circuit is coupled to the load resistor center  
4 tap of the third comparator circuit to provide the first and second comparator circuits  
5 with symmetrical offsets.

1           16.    The integrated circuit of claim 13 wherein the first and third thresholds  
2 of the data slicer are equally spaced from the second threshold.

1           17.    The integrated circuit of claim 13 wherein the comparator circuits are  
2 formed from complimentary metal oxide semiconductor devices.